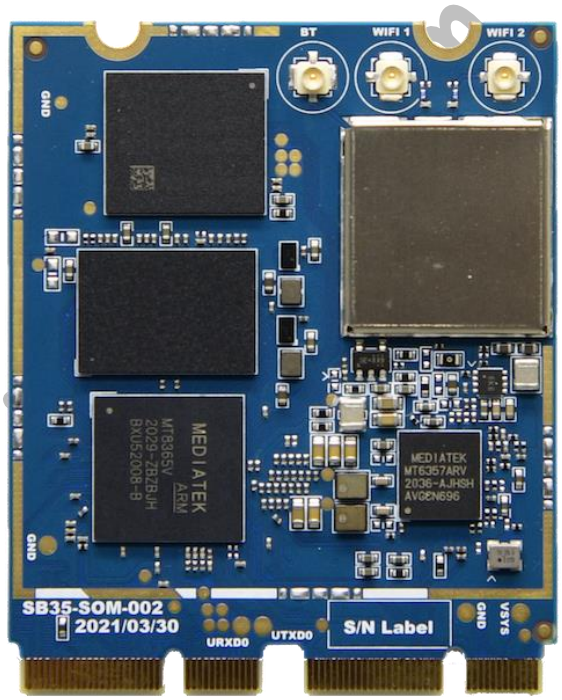
SB35 SOM

Datasheet



Revisions History

Date	Version Number	Document Changes
2021/04/27	0.1	Initial Draft
2021/6/4	1.0	Update content and diagrams
2022/3/17	2.0	Pin definition modification
2022/11/16	2.1	Updated DSI interface operating resolution
2023/06/08	2.2	Updated the operating temperature lower limit to -10℃

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1 Overview

1.1 General Information

SB35 SOM is a high-performance System on Module(SOM) designed based on the i350 processor from MediaTek. The i350 device, with integrated Bluetooth, and WLAN modules, is a highly integrated baseband platform incorporating application processing subsystems. The chip integrates ARM®Cortex-A53 MPCore operating up to 2GHz, AI Processor MediaTek APU 1.0, and a powerful multi-standard video codec.

The application processor, a Quad-core ARM® Cortex-A53 MPCore equipped with the NEON engine offers the processing power necessary to support the latest Open OS along with its demanding applications such as web browsing, email, and games. All are viewed on a high-resolution touch screen display with graphics enhanced by the 2D and 3D graphics acceleration. The multi-standard video accelerator and an advanced audio subsystem are also integrations and services such as streaming and encoders.

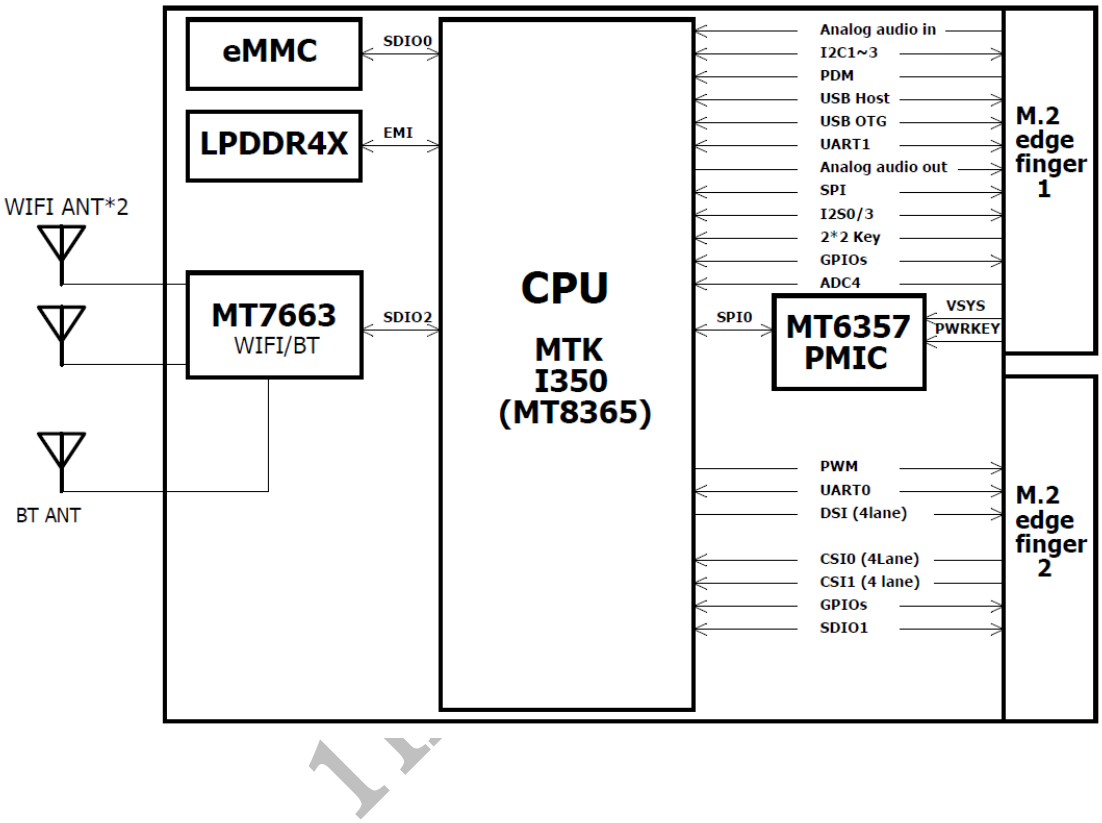
AI Processor Unit System is a highly efficient computing unit system which is most suitable for AI/CV algorithms. It includes one programmable AI processor (Cadence VP6) for both AI and CV algorithms, and an eDMA engine for data movement between DRAM and VP6 internal memory. The maximum operation frequency of VP6 is 700MHz at 0.825V.

SB35 also embodies wireless communication devices, including WLAN and Bluetooth. The RF part is a built-in MT7663 chip that can support dual-band (2.4GHz and 5GHz) 802.11 a/b/g/n/ac WLAN. It also supports one dedicated antenna for Bluetooth and two 2.4GHz/5GHz dual band antennas for WLAN.

SB35 SOM offers a wide range of interfaces - GPIOs, I2S, I2C, SPI, DSI, CSI, ADC, UART, USB, Audio out, PWM.

1.2 Architecture and Block Diagram

Figure 1-1 SB35 SOM Block Diagram



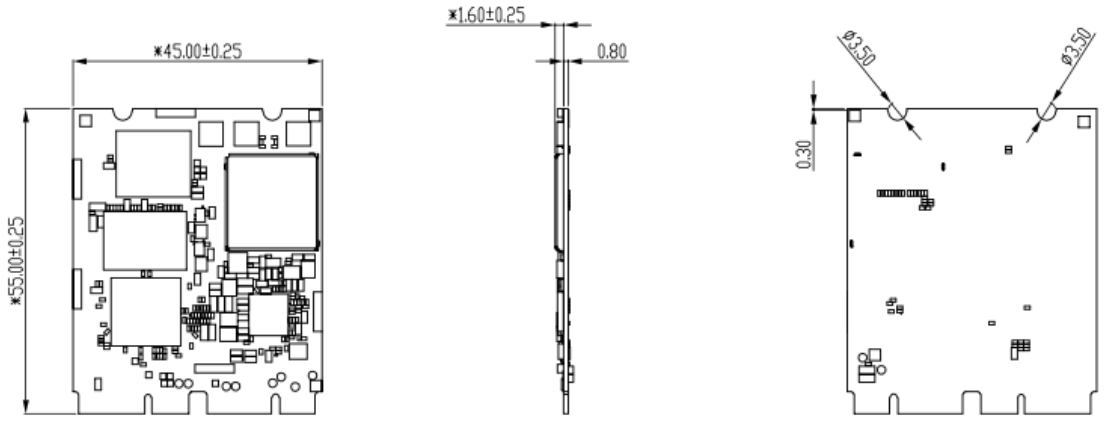
1.3 Feature Summary

- MTK i350 CPU
- 2/4GB LPDDR4X RAM
- 16/32GB eMMC
- 1 x MIPI DSI (4 data lanes)
- 2 x MIPI CSI (4 data lanes)
- Wi-Fi 802.11 a/b/g/n/ac, MIMO (MT7663)
- Bluetooth 5.1 (MT7663)
- 1 x USB 2.0 OTG,1 x USB 2.0 Host
- Serial interfaces (3 x I2C, 2 x UART, 1 x SPI, 2 x I2S)
- GPIOs pin-mux with serial interfaces
- Earphone interface, R/L channel output and microphone input
- 1x ADC

1.4 Dimension

The dimension of SB35 is 55 mm x 45 mm x 3.5 mm. Detail dimension please see Fig1-2.

Figure 1-2 SB35 SOM Dimension



1.5 Electrical Specifications

Symbol	Parameter	Minimum	Maximum	Unit
VSYS	Input Voltage	3.4	4.35	V
VSYS	Input Current		1.5	A

Table 1-1: Input Power Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
VIO28_PMU	VDDIO_2V8	2.66	2.94	V
VIO18_PMU	VDDIO_1V8	1.71	1.89	V

Table 1-2: Output Power

Symbol	Parameter	Minimum	Maximum	Unit
T	Operating Temp.	-10	65 *	℃

Table 1-3 Operating Temperature

Note * : Test with heat sink

1.6 General Application Notes

Consider the following recommendations when designing application boards:

- Use a GND plane underneath the SB35.
- Do not use vias in high-speed interface lines such as USB and Ethernet.
- Rout high-speed interface lines differentially and leave a several mm gap to other signal lines when possible.
- Do not place any components which dissipate heat close to or underneath the module.
- A heat sink is suggested to allow prolonged operation under full CPU speed. Connect heatsink to CPU and WiFi via thermal pad, ensure that heatsink is not tilted or applying high force onto the module.

2 Main Hardware Components

SB35 SOM has two 75-pin M.2 E-key golden fingers to connect with carrier board. It integrates MTK the i350, LPDDR4 Memory, eMMC, Power Manage IC (PMIC), and Wi-Fi/Bluetooth on the module.

Figure 2-1 – Top side of SB35 SOM

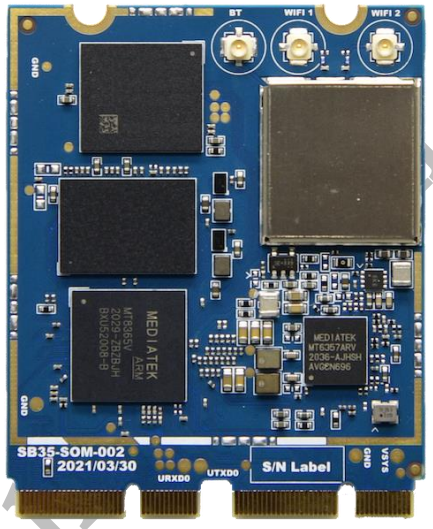
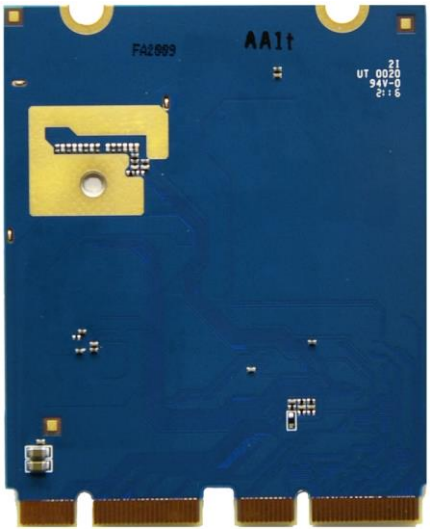


Figure 2-2 – Bottom side of SB35 SOM



2.1 Processor

MTK i350 processor integrates a Quad-core ARM® Cortex-A53 MPCore equipped with the NEON engine offers processing power necessary to support the latest Open OS along with its demanding applications such as web browsing, email, and games.

The features of i350 processors include the following:

- Quad-core ARM Cortex-A53MPCore operating at 2GHz
- NEON multimedia processing engine
- ARM TrustZone security
- MediaTek APU 1.0 (AI Processor)

2.2 Memory

SB35 SOM is embedded LPDDR4X memory with the following feature,

- Dual channels with a 16-bit data bus width
- Up to 3200MHz memory clock
- Supports self-refresh/ partial self-refresh mode
- Advanced bandwidth arbitration control

2.3 Power Management IC

MTK MT6357 power management IC is used for SB35 SOM. MT6357 is a programmable power management IC that integrates 5 buck converters and 29 LDOs to provide all power rails required by SoC and peripherals.

MT6357 adopts the SPI interface and two SRCLKEN control pins to control buck converters, LDOs, and various drivers; it provides enhanced safety control and protocol for handshaking with i350.

For system management, it provides the following features,

- Support software shutdown or hardware power off
- 32K RTC oscillator for system timing
- Watchdog reset
- Over-current and thermal overload protection
- OVP, UVLO function
- Precision voltage, temperature, and current measurement fuel gauge

2.4 eMMC Storage

The onboard eMMC device is connected to the MSDC0 interface of the i350 processor in an 8-bit width configuration.

2.5 Wi-Fi/Bluetooth Module

MTK MT7663 WIFI/BT IC is used for SB35. It supports Wi-Fi 802.11 a/b/g/n/ac MIMO and BT5.1.

3 SB35 SOM Interfaces and Connectors

SB35 use two M.2 E-key golden finger to connect with the carrier board. The tables below detail the pin assignment and functionality of these connectors.

3.1 J101 Connector

Table 3-1 J101 Connector

J101 Pin#	Signal Name	I350 Pin #	MT6357 Pin #	I/O	Voltage (V)
1	SYSRSTB	AC30	R5	I	1.8
2	VSYS			PI	3.4 ~ 4.35
3	PWRKEY		R4	I	0 ~ 5
4	VSYS			PI	3.4 ~ 4.35
5	VIO28_PMU		K15	PO	2.8
6	VSYS			PI	3.4 ~ 4.35
7	GND				
8	VSYS			PI	3.4 ~ 4.35
9	GND				
10	GND				
11	AUXIN4	AC18		AI	0 ~ 1.45
12	VBUS (VCDT)	V30	T11	PI	5
13	GPIO13	AE16		I/O	1.8
14	VRTC28		R12	PO	2.8
15	GPIO7	AG21		I/O	1.8
16	I2S0_MCK	AF2		I/O	1.8
17	UCTS1	AE24		I/O	1.8
18	I2S0_BCK	AE3		I/O	1.8
19	SDA3	AD5		OD	1.8
20	I2S0_LRCK	AF1		I/O	1.8
21	SCL3	AC5		OD	1.8
22	I2S0_DI	AG2		I/O	1.8
23	MICBIAS0		L3	PO	1.7~2.6

J101 Pin#	Signal Name	I350 Pin #	MT6357 Pin #	I/O	Voltage
32	SPI_CS	AG18		I/O	1.8
33	DMIC0_DAT1	AE30		I	1.8
34	SPI_CK	AJ19		I/O	1.8
35	DMIC0_CLK	AD29		I	1.8
36	SPI_MI	AJ18		I/O	1.8
37	DMIC0_DAT0	AC29		I	1.8
38	SPI_MO	AH18		I/O	1.8
39	AU_REFN		H3	AGND	
40	URTS1	AE23		I/O	1.8
41	AU_HPR		G3	AO	-1.98 ~ 1.98
42	GPIO4	AF19		I/O	1.8
43	AU_HPL		J2	AO	-1.98 ~ 1.98
44	I2S3_MCK	AJ25		I/O	1.8
45	GND			GND	
46	I2S3_LRCK	AF27		I/O	1.8
47	MICBIAS1		M3	O	1.7~2.6
48	I2S3_BCK	AF26		I/O	1.8
49	AU_VIN1_P		K5	I	MICBIAS
50	I2S3_DO	AH25		I/O	1.8
51	AU_VIN1_N		L5	I	MICBIAS
52	KPROW0	AD24		I/O	1.8
53	ACCDET		M4	I	0 ~ 2.94V
54	URXD1	AF22		I/O	1.8
55	HP_EINT		J1	I	0 ~ 2.94V
56	UTXD1	AF23		I/O	1.8
57	GND			GND	
58	KPCOL0	AA24		I/O	1.8
59	USB_DM_P0	T29		USB	
60	KPROW1	AB24		I/O	1.8
61	USB_DP_P0	T30		USB	
62	KPCOL1	AC24		I/O	1.8
63	GND			GND	
64	SDA2	AJ4		I/O	1.8
65	USB_DM_P1	T25		USB	
66	SCL2	AH4		I/O	1.8

J101 Pin#	Signal Name	I350 Pin #	MT6357 Pin #	I/O	Voltage
67	USB_DP_P1	T26		USB	
68	GPIO16	AH17		I/O	1.8
69	GND			GND	
70	GPIO123	AF29		I/O	1.8
71	SDA1	AJ24		I/O	1.8
72	GPIO124	AH29		I/O	1.8
73	SCL1	AH24		I/O	1.8
74	GPIO125	AG29		I/O	1.8
75	VIO18_PMU		B17	PO	1.8

3.2 J102 Connector

Table 3-2 J102 Connector

J102 Pin#	Signal Name	I350 Pin #	MT6357 Pin #	I/O	Voltage
1	AVSS28_AUD		H5	AGND	
2	VLDO28_PMU		L16	PO	2.8/3
3	GND			GND	
4	GPIO20	AB4		I/O	1.8
5	URXD0	AH22		I/O	1.8
6	DISP_PWM	AB5		I/O	1.8
7	UTXD0	AH23		I/O	1.8
8	DISP_TE	AA5		I/O	1.8
9	FCHR_ENB		N4	I	1.8
10	GPIO0	AE20		I/O	1.8
11	IDDIG	AH16		I/O	1.8
12	GPIO1	AE21		I/O	1.8
13	GPIO14	AF17		I/O	1.8
14	GPIO2	AF21		I/O	1.8
15	GPIO15	AG17		I/O	1.8
16	GPIO3	AG22		I/O	1.8
17	DSI_D2N	Y6		DSI	
18	GPIO5	AH19		I/O	1.8

J102 Pin#	Signal Name	I350 Pin #	MT6357 Pin #	I/O	Voltage
19	DSI_D2P	W6		DSI	
20	DSI_D3N	AC2		DSI	
21	DSI_D1N	AA2		DSI	
22	DSI_D3P	AC3		DSI	
23	DSI_D1P	AB2		DSI	
32	DSI_CKP	AA3		DSI	
33	DSI_D0N	W4		DSI	
34	DSI_CKN	Y3		DSI	
35	DSI_D0P	W5		DSI	
36	CMMCLK0	AD4		I/O	1.8
37	RDN3_0	T2		CSI	
38	RDN2_0	R3		CSI	
39	RDP3_0	R2		CSI	
40	RDP2_0	R4		CSI	
41	RDN1_0	U1		CSI	
42	RCP_0	P7		CSI	
43	RDP1_0	T1		CSI	
44	RCN_0	P6		CSI	
45	RDN0_0	P4		CSI	
46	GND			GND	
47	RDP0_0	P5		CSI	
48	RDN3_1	V2		CSI	
49	GND			GND	
50	RDP3_1	U2		CSI	
51	VCAMA_PMU		H16	PO	1.8/2.5/2.7/ 2.8/2.9/3
52	RDN2_1	U5		CSI	
53	VCAMD_PMU		E17	PO	0.9/1.0/1.05/1.1 /1.2/1.3/1.5/1.8
54	RDP2_1	U6		CSI	
55	VCAMIO_PMU		A17	PO	1.8
56	GPIO6	AF18		I/O	1.8
57	GPIO12	AE17		I/O	1.8

J102 Pin#	Signal Name	I350 Pin #	MT6357 Pin #	I/O	Voltage
58	GND			GND	
59	RCP_1	R7		CSI	
60	MSDC1_INSI	AH1		I/O	1.8
61	RCN_1	R6		CSI	
62	VMCH_PMU		N16	PO	2.9/3.0/3.3
63	GND			GND	
64	MSDC1_CMD	M6		I/O	1.8
65	CAMCLK1	AE4		I/O	1.8
66	MSDC1_CLK	M3		I/O	1.8
67	GND			GND	
68	MSDC1_DAT0	L3		I/O	1.8
69	RDN1_1	W1		CSI	
70	MSDC1_DAT1	L2		I/O	1.8
71	RDP1_1	W2		CSI	
72	MSDC1_DAT2	M4		I/O	1.8
73	RDN0_1	T3		CSI	
74	MSDC1_DAT3	M5		I/O	1.8
75	RDP0_1	T4		CSI	

3.3 Power Signals

Table 3-3 Power Signal Pins

Connector#	PIN#	Function	I/O	Description
J101	2,4,6,8	VSYS	I	Input power 3.4 ~ 4.35V
J101	14	VRTC28	I/O	RTC power 2.8V
J101	5	VCAMA2_PMU	O	Camera2 power 2.8V
J101	23	AU_MICBIAS0	O	Microphone0 Bias power 1.7~2.6V
J101	47	AU_MICBIAS1	O	Microphone1 Bias power 1.7~2.6V
J101	75	VIO18_PMU	O	IO power 1.8V
J102	51	VCAMA_PMU	O	Camera1 power 2.8V
J102	53	VCAMD_PMU	O	Camera1 power 1.2V
J102	55	VCAMIO_PMU	O	Camera1 power 1.8V
J102	2	VLDO28_PMU	O	IO power 2.8V
J102	62	VMCH_PMU	O	IO power 3.3V

3.4 I2CsParameter Specification

SB35 SOM I2C is an open-drain interface, the specification is shown in Table 3-5.

Table 3-4 I2C parameter specification

Parameters	Description	Min	Typ	Max	Unit
VIH	Input logic high voltage	0.65*VDD		VDD+0.3	V
VIL	Input logic low voltage	-0.3		0.35*VDD	V
VOL	DC output low voltage			0.2*VDD	V

*VDD is 1.8V

Table 3-5 I2C Signal Pins

Connector#	PIN#	PIN name	I/O	Description
J101	71	SDA1	OD*	I2C1_SDA
J101	73	SCL1	OD*	I2C1_SCL
J101	64	SDA2	OD*	I2C2_SDA
J101	66	SCL2	OD*	I2C2_SCL
J101	19	SDA3	OD*	I2C3_SDA
J101	21	SCL3	OD*	I2C3_SCL

* OD is Open drain

3.5 UARTs

SB35 supports two UARTs. UART0 is not recommended to use since this port is default for debug trace log function. UART1 has HW flow control with another two control pins for CTS and RTS function.

Table 3-6 UART Signal Pins

Connector#	PIN#	PIN name	I/O	Description
J102	5	URXD0	I	UART0_RXD
J102	7	UTXD0	O	UART0_TXD
J101	54	URXD1	I	UART1_RXD
J101	56	UTXD1	O	UART1_TXD
J101	17	UCTS1	I	UART1_CTS
J101	40	URTS1	O	UART1_RTS

3.6 DSI Interface

SB35 SOM provides a 4-lanes MIPI DSI display interface operating up to 1920*1200 resolution.

Table 3-7 DSI Signal Pins

Connector#	PIN#	PIN name	I/O	Description
J102	33	DSI_D0N	O	DSI_D0M
J102	35	DSI_D0P	O	DSI_D0P
J102	21	DSI_D1N	O	DSI_D1M
J102	23	DSI_D1P	O	DSI_D1P
J102	17	DSI_D2N	O	DSI_D2M
J102	19	DSI_D2P	O	DSI_D2P
J102	20	DSI_D3N	O	DSI_D3M
J102	22	DSI_D3P	O	DSI_D3P
J102	34	DSI_CKN	O	DSI_CLKM
J102	32	DSI_CKP	O	DSI_CLKP

3.7 CSI Interface

SB35 SOM provides 2 MIPI CSI high-speed camera serial interface with 4 data lane (for main and sub) and throughput up to 1.5G bps for 1 data lane.

Table 3-8 CSI0 Signal Pins

Connector#	PIN#	PIN name	I/O	Description
J102	47	RDP0_0	I	CSI0_D0P
J102	45	RDN0_0	I	CSI0_D0M
J102	43	RDP1_0	I	CSI0_D1P
J102	41	RDN1_0	I	CSI0_D1M
J102	40	RDP2_0	I	CSI0_D2P
J102	38	RDN2_0	I	CSI0_D2M
J102	39	RDP3_0	I	CSI0_D3P
J102	37	RDN3_0	I	CSI0_D3M
J102	42	RCP_0	I	CSI0_CLKP
J102	44	RCN_0	I	CSI0_CLKM

Table 3-9 CSI1 Signal Pins

Connector#	PIN#	PIN name	I/O	Description
J102	75	RDP0_1	I	CSI1_D0P
J102	73	RDN0_1	I	CSI1_D0M
J102	71	RDP1_1	I	CSI1_D1P
J102	69	RDN1_1	I	CSI1_D1M
J102	54	RDP2_1	I	CSI1_D2P
J102	52	RDN2_1	I	CSI1_D2M
J102	50	RDP3_1	I	CSI1_D3P
J102	48	RDN3_1	I	CSI1_D3M
J102	59	RCP_1	I	CSI1_CLKP
J102	61	RCN_1	I	CSI1_CLKM

3.8 Audio

SB35 SOM provides 2 I2S input/output interface and 2 PDM interface from I350, 1 earphone interface from MT6357.

SB35 SOM supports I2S audio interface with below feature,

- Audio content sampling rates supported: 8kHz to 192kHz
- Audio content sample formats supported: 8-bit/16-bit/24-bit, Mono/stereo
- Interface supported: I2S, PCM, TDM TX/RX
- External CODEC I2S interface supports 16-bit/24-bit, Mono/Stereo, 8kHz to 192kHz

Table 3-10 I2S Signal Pins

Connector#	PIN#	PIN name	I/O	Description
J101	20	I2S0_LRCK	O	I2S LRCK
J101	18	I2S0_BCK	O	I2S BCK
J101	22	I2S0_DI	I	I2S DI
J101	16	I2S0_MCK	O	I2S MCLK
J101	46	I2S3_LRCK	I	I2S LRCK
J101	48	I2S3_BCK		I2S BCK
J101	50	I2S3_DO		I2S DO
J101	44	I2S3_MCK		I2S MCLK

Table 3-11 other Audio Signal Pins

Connector#	PIN#	PIN name	I/O	Description
J101	35	DMIC0_CLK	O	PDM for DMIC
J101	37	DMIC0_DAT0	I	PDM for DMIC
J101	33	DMIC0_DAT1	I	PDM for DMIC
J101	49	AU_VIN1_P	I	earphone MIC input
J101	51	AU_VIN1_N	I	earphone MIC input
J101	39	AU_REFN	GND	earphone line out reference GND
J101	41	AU_HPR	O	earphone line out
J101	43	AU_HPL	O	earphone line out
J101	53	ACCDET	I	Accessory detection input
J101	55	HP_EINT	I	HPL detection

3.9 USB

SB35 SOM provides 2 high-speed USB functionality conforms to the USB2.0 (1xOTG mode, 1xHost mode) . The OTG controller conforms to OTG2.0 specification.

Table 3-12 USB Signal Pins

Connector#	PIN#	PIN name	I/O	Description
J101	61	USB_DP_P0	I/0	USB0 DP
J101	59	USB_DM_P0	I/0	USB0 DM
J102	11	IDDIG	I	USB ID
J101	12	VBUS	P	USB VBUS
J101	67	USB_DP_P1	I/0	USB1 DP
J101	65	USB_DM_P1	I/0	USB1 DM

3.10 GPIO

All the IOs from i350 can be configured to GPIO purposes. For more detail pin-mux table please see the reference documents [1].

4 Reference Documents

1. MT8365_AIoT Application Processor Functional Specification
2. MT6357_PMIC_Data_Sheet
3. MT7663_Datasheet